TECHNICAL DOCUMENT

HyperTransport™ CONSORTIUM

HyperTransport™ Consortium

HyperTransport™ EATX Motherboard/Daughtercard Specification

Including Errata Revision C

Connector and Form Factor Specification for HyperTransport™ Daughtercards and EATX Motherboards

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-	Initial Release		10/04
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0006	Vote passed to release Errata C (two typos in Figure 6)		10/12/05

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1. Objective

The HyperTransport™ EATX Motherboard/Daughtercard Specification allows system developers to deliver HyperTransport™ solutions using standard high-volume platforms such as Opteron™ servers. Standardized HyperTransport™-enabled motherboards will enable HyperTransport™ silicon and subsystem developers to deliver solutions based on commodity hardware—eliminating the need for custom solutions on most cases.

2. Electrical Features of the Specification

The HyperTransport™ EATX Motherboard/Daughtercard Specification:

- Supports a 16-bit HyperTransport™ interface
- Daughtercards may choose to implement only 8 bits
- Runs at up to an 800MHz clock (1.6G transfers/sec). (Support for higher clock speeds is outside of the scope of this specification.)
- Provides all HyperTransport™-specific control signals, including synchronous reference clock
- Delivers both 12V and 3.3V power, up to 63 watts combined
- Provides an SMBus interface (3.3V)
- Optionally supports JTAG
- Allows use of 4-layer motherboards and daughtercards with conventional PCB technology

3. Mechanical Features of the Specification

The HyperTransport™ EATX Motherboard/Daughtercard Specification:

- Is optionally compatible with the standard Extended ATX (12x13”) motherboard form factor
- Daughtercard mechanical envelope is compatible with standard PCI cards to fit in existing chassis designs
- Usable in both riser-based (1U) and pedestal, rack-mount (3U and greater) or proprietary applications
- Uses an inexpensive, multiply-sourced commodity connector
- Placement of connectors designed to exclude the possibility of accidentally inserting cards built to other known interface specifications

4. Specification Summary

A typical HyperTransport™ dual-processor motherboard layout is illustrated in Figure 1. The slots are numbered from right to left as is the convention for extended ATX. The HyperTransport™ connectors occupy slot 6, utilizing standard PCI-Express™ 1x and 16x connectors installed in the reverse orientation of normal PCI-Express™. Slot 6 results in a design which is the most easily routable, has the shortest and most direct path for HyperTransport™, and which allows the same form factor as PCI in a 1U server. Note that the HyperTransport™ signals should route in from the right side so that the signals have the correct routing order on the daughtercard's HyperTransport™ chip. The HyperTransport™ host must reside on the motherboard.

The rest of the board's I/O infrastructure is unaffected. The function of slots 1 through 5 is application-dependent and beyond the scope of this document.

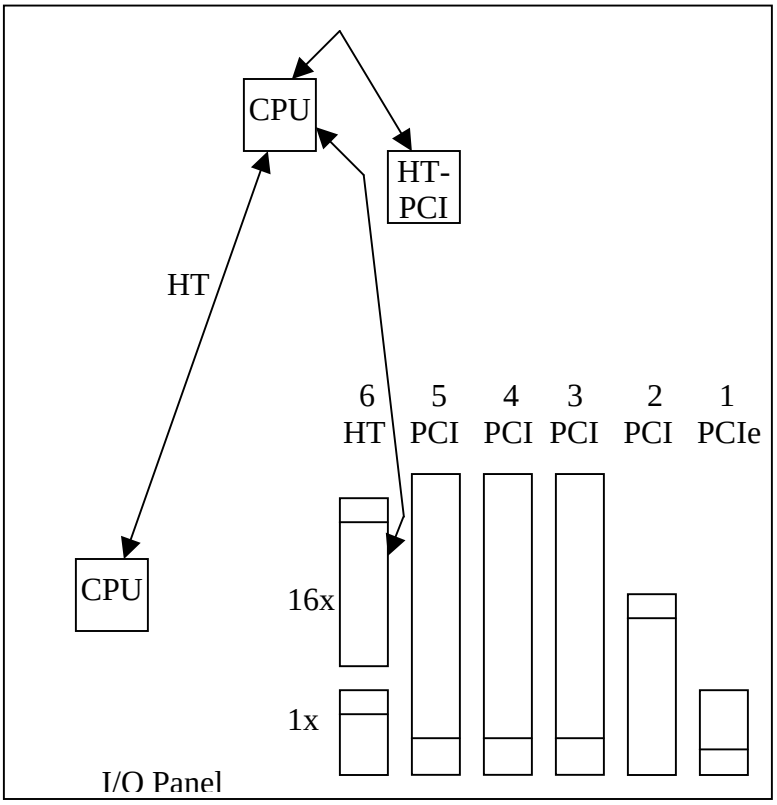

Figure 1. Typical Dual Processor HyperTransport™ Motherboard

This specification defines the mechanical locations of the connectors, pinouts, signaling conventions, mechanical specifications for the 1U riser card and HyperTransport™ daughtercard, and layout rules for motherboard, riser, and daughtercard.

A 1U system, shown in Figure 2, supports a single HyperTransport™ daughtercard using the HyperTransport™ riser, and such a HyperTransport™-enabled assembly is mechanically 100% compatible with existing 1U chassis designs.

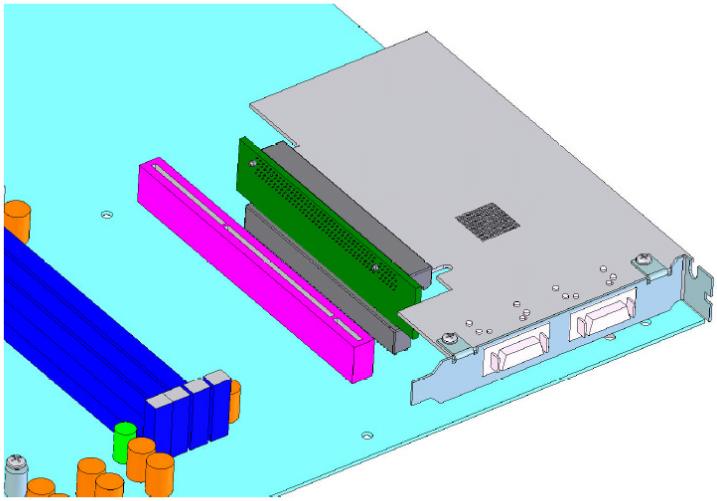

Figure 2. 1U System with Riser

A 3U or greater rack-mount or pedestal server can accommodate the card plugged in vertically in conjunction with other PCI and/or PCI Express™ cards, as shown in Figure 3. No change in chassis design is required.

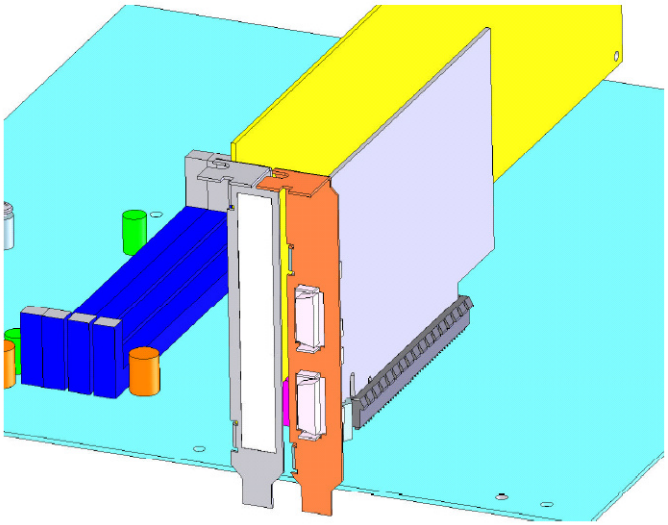

Figure 3. 3U System with Vertically Mounted HT Daughtercard

5. Connector Pinout

Pinouts for the two HyperTransport™ motherboard connectors are shown in Figure 4. Signal names are from the perspective of the motherboard, e.g. the motherboard drives CADOUT signals and receives CADIN signals, etc.

Figure 4. Connector pinouts:

Pin	A	B	Pin
1	RSVD	GND	1
2	VLDT	GND	2
3	GND	CADIN8H	3
4	GND	CADIN8L	4
5	CADIN0H	GND	5
6	CADIN0L	GND	6
7	GND	CADIN9H	7
8	GND	CADIN9L	8
9	CADIN1H	GND	9
10	CADIN1L	GND	10
11	GND	RSVD	11
12	RSVD	GND	12
13	GND	CADIN10H	13
14	GND	CADIN10L	14
15	CADIN2H	GND	15
16	CADIN2L	GND	16
17	GND	CADIN11H	17
18	GND	CADIN11L	18
19	CADIN3H	GND	19
20	CADIN3L	GND	20
21	GND	CLKIN1H	21
22	GND	CLKIN1L	22
23	CLKIN0H	GND	23
24	CLKIN0L	GND	24
25	GND	CADIN12H	25
26	GND	CADIN12L	26
27	CADIN4H	GND	27
28	CADIN4L	GND	28
29	GND	CADIN13H	29
30	GND	CADIN13L	30
31	CADIN5H	GND	31
32	CADIN5L	GND	32
33	GND	CADIN14H	33
34	GND	CADIN14L	34
35	CADIN6H	GND	35
36	CADIN6L	GND	36
37	GND	CADIN15H	37
38	GND	CADIN15L	38
39	CADIN7H	GND	39
40	CADIN7L	GND	40
41	GND	CTLINH	41
42	GND	CTLINL	42
43	CTLOUTL	GND	43
44	CTLOUTH	GND	44
45	GND	CADOUT15L	45
46	GND	CADOUT15H	46
47	CADOUT7L	GND	47
48	CADOUT7H	GND	48
49	GND	CADOUT14L	49
50	GND	CADOUT14H	50
51	CADOUT6L	GND	51

Top of connector, away from I/O Panel as viewed from the solder side of the motherboard.

52	CADOUT6H	GND	52
53	GND	CADOUT13L	53
54	GND	CADOUT13H	54
55	CADOUT5L	GND	55
56	CADOUT5H	GND	56
57	GND	CADOUT12L	57
58	GND	CADOUT12H	58
59	CADOUT4L	GND	59
60	CADOUT4H	GND	60
61	GND	CLKOUT1L	61
62	GND	CLKOUT1H	62
63	CLKOUT0L	GND	63
64	CLKOUT0H	GND	64
65	GND	CADOUT11L	65
66	GND	CADOUT11H	66
67	CADOUT3L	GND	67
68	CADOUT3H	GND	68
69	GND	CADOUT10L	69
70	GND	CADOUT10H	70
71	CADOUT2L	GND	71
72	CADOUT2H	GND	72
73	GND	CADOUT9L	73
74	GND	CADOUT9H	74
75	CADOUT1L	GND	75
76	CADOUT1H	GND	76
77	GND	CADOUT8L	77
78	GND	CADOUT8H	78
79	CADOUT0L	GND	79
80	CADOUT0H	GND	80
81	GND	USER	81
82	RSVD	GND	82

Pin	A	B	Pin
1	GND	REFCLK66	1
2	REFCLKL	GND	2
3	REFCLKH	GND	3
4	GND	USER	4
5	GND	USER	5
6	USER	GND	6
7	RSVD	PWROK	7
8	LDTSTOP#	RESET#	8
9	+3.3Vaux	+3.3V	9
10	TRST#	+3.3V	10
11	+3.3V	TMS	11
12	GND	TDO	12
13	SMDAT	TDI	13
14	SMCLK	TCK	14
15	GND	GND	15
16	RSVDFS	+12V	16
17	+12V	+12V	17
18	+12V	RSVDFS	18

Bottom of connector, near I/O panel

Unshaded pins are staggered closer together in the connector than shaded pins.

Pinout considerations include:

- No high-speed signals at connector edge
- Dedicated ground next to every high-speed signal
- HyperTransport™-specific control and power signals closer to top of connector
- Ordering of HyperTransport™ interface matches standard device pinout
- Pinout near I/O panel similar to PCI-Express™ pinout for ease of bussing

6. Power distribution

Power specifications, shown in Figure 5, are identical to 16x PCI-Express™ with the addition of VLDT.

Power supply	Voltage	Tolerance	Current
+12V	12V	±8%	4.4A
+3.3V	3.3V	±9%	3A
+3.3Vaux	3.3V	±9%	375ma
VLDT	1.2V	±5%	1A

Figure 5. Power specifications

7. Signal Description Summary

Figure 6 provides a description of the signals on the HyperTransport™ connectors. "MB" refers to motherboard and "DC" refers to daughtercard.

Figure 6. Connector Signal Characteristics

Signal name	Count	Direction	Level	Description	Required MB	Required DC
+12V	4	In	Power	12V power	Yes	Yes
+3.3V	3	In	Power	3.3V power	Yes	Yes
+3.3Vaux	1	In	Power	3.3V auxiliary power	Yes	Yes
VLDT	1	In	Power	1.2V HT power	Yes	Yes
GND	91	Common	Ground	Signal ground	Yes	Yes
CADIN[15:8][H:L]	8 pairs	DC→MB	LDT diff	HT data/command	Yes	No
CADIN[7:0][H:L]	8 pairs	DC→MB	LDT diff	HT data/command	Yes	Yes
CLKIN1[H:L]	1 pair	DC→MB	LDT diff	HT clock	Yes	No
CLKIN0[H:L]	1 pair	DC→MB	LDT diff	HT clock	Yes	Yes
CTLIN[H:L]	1 pair	DC→MB	LDT diff	HT control	Yes	Yes
CADOUT[15:8][H:L]	8 pairs	MB→DC	LDT diff	HT data/command	Yes	No
CADOUT[7:0][H:L]	8 pairs	MB→DC	LDT diff	HT data/command	Yes	Yes
CLKOUT1[H:L]	1 pair	MB→DC	LDT diff	HT clock	Yes	No
CLKOUT0[H:L]	1 pair	MB→DC	LDT diff	HT clock	Yes	Yes
CTLOUT[H:L]	1 pair	MB→DC	LDT diff	HT control	Yes	Yes
LDTSTOP#	1	MB→DC	2.5V CMOS	HT LDTSTOP	Yes	Yes
PWROK	1	MB→DC	2.5V CMOS	HT power OK	Yes	Yes
RESET#	1	Bidir	2.5V CMOS	HT reset	Yes	Yes
REFCLK[H:L]	1 pair	MB→DC	2.5V diff	200MHz HT reference clock	Yes	Yes
REFCLK66	1	MB→DC	3.3V CMOS	66 MHz reference clock	Yes	No
SMCLK	1	MB→DC	3.3V CMOS	SMBus clock	Yes	No
SMDAT	1	Bidir	3.3V CMOS	SMBus data	Yes	No
TCK	1	MB→DC	3.3V CMOS	JTAG clock	No	No
TMS	1	MB→DC	3.3V CMOS	JTAG mode select	No	No
TRST#	1	MB→DC	3.3V CMOS	JTAG reset	No	No
TDI	1	MB→DC	3.3V CMOS	JTAG data in	No	No
TDO	1	DC→MB	3.3V CMOS	JTAG data out	No	No
USER	4	User	User	User-defined	-	-
RSVD	5	-	-	Reserved, do not connect	-	-
RSVDFS	2	-	-	Reserved, future standardization	-	-

8. Routing Rules

The HyperTransport™ connector should be considered a “zero mismatch boundary” as defined in Section 2.3.6.2 of the HyperTransport™ Interface Design Guide, Rev. 1.07. Motherboard and daughtercard routing should comply with the Interface Design Guide using this assumption. This allows the routing for the motherboard and the daughtercard to be independent and interoperable.

Trace lengths for HyperTransport™ signals on the motherboard should not exceed 9.25 inches. Trace lengths on the daughtercard should not exceed 2.75 inches. This will ensure that the total trace length will not exceed the maximum allowed 12 inches for 800 MT/sec operation.

9. Signal Integrity

Signal integrity shall be measured according to the HyperTransport™ Electrical Compatibility Measurements Rev. 0.03, HyperTransport Technology Consortium document number HTC20021219-0018-0001.pdf, and shall be compliant with the HyperTransport I/O Link Specification, Rev. 2.0.

10. Higher Speed Operation

Operation at speeds higher than 800 MT/sec is outside the scope of this specification. However, the connectors used are known to work at higher speeds in PCI-Express™ applications. Designers are urged to minimize trace lengths and signal skew to achieve best results at higher speeds.

11. 8-bit Link Support

If a daughtercard only supports an 8-bit HyperTransport link, then it must tie CADIN[15:8]H and CLKIN1H to GND through 51 ohm resistors and CADIN[15:8]L and CLKIN1L to VLDT through 51 ohm resistors.

12. Unused HyperTransport Slot

In the event that the HyperTransport™ slot is unused, an optional terminator board of the same form factor as the HyperTransport™ daughtercard or the same form factor as the HyperTransport™ riser card may be provided to prevent floating inputs and/or jumper the JTAG chain. This board should tie CADIN[15:0]H, CLKIN[1:0]H and CTLINH to GND through 51 ohm resistors and CADIN[15:0]L, CLKIN[1:0]L and CTLINL to VLDT through 51 ohm resistors. TDI should be jumpered to TDO to complete the JTAG chain.

13. Motherboard Dimensions and Connector Placement

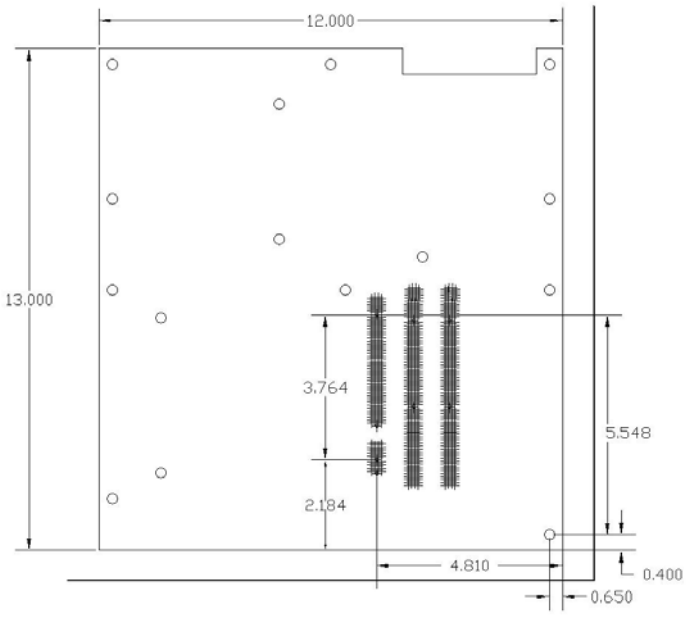

Figure 7. EATX Motherboard with HyperTranport™ Connector in Slot 6 Position

The example shown in Figure 7 is an EATX motherboard with the HyperTransport™ connector in the position normally occupied by PCI slot 6. Placing the HyperTransport™ connector in the slot 6 position permits operation with a riser, allowing the use of a 1u enclosure. Proprietary designs or motherboards designed for use in a 3u or greater enclosure may place the HyperTransport™ connector in any of the PCI slot positions provided that HT layout and signal integrity requirements are met.

14. Riser Dimensions

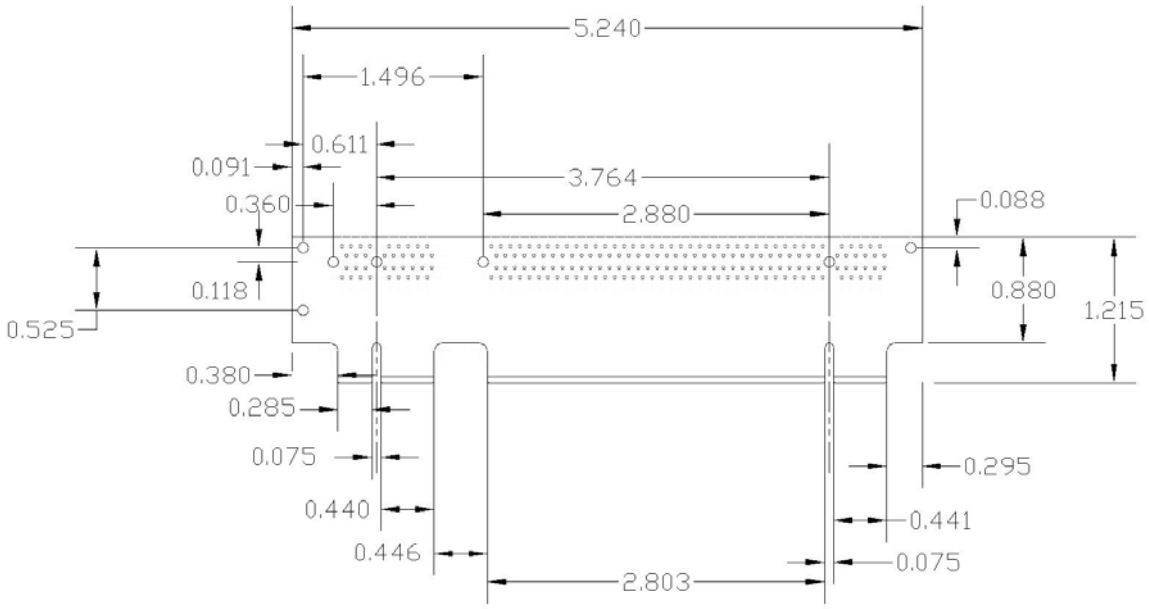

Figure 8. HT Riser for 1U Systems

The riser card allows operation of the HyperTransport daughtercard in 1U chassis. Care should be taken to ensure that the HyperTransport traces on the riser card are of equal length so that the effect of the riser on HyperTransport™ signal-to-signal skew is minimized. Bypass capacitors should be added between the +12V and +3.3V power planes and ground to reduce power supply ripple and noise. It is recommended that two 220uF electrolytic capacitors be used to bypass +12V and two 470uF electrolytic capacitors be used to bypass +3.3V.

15. Daughtercard Dimensions

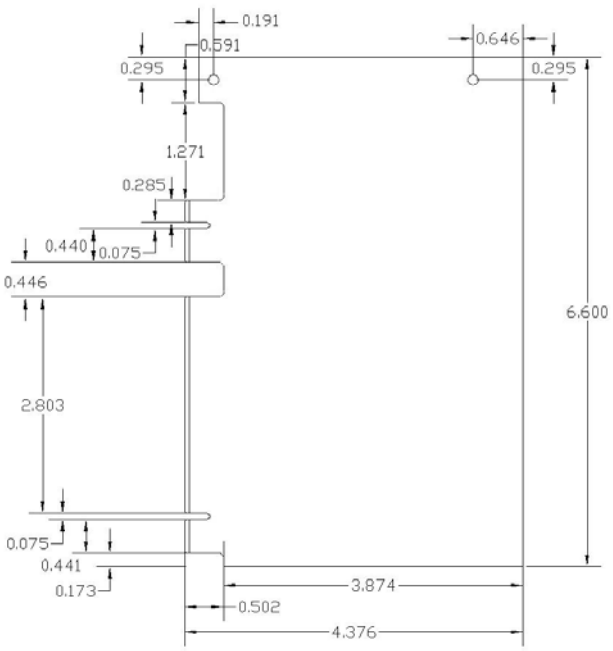

Figure 9. Daughtercard Outline

Figure 9 shows the mechanical outline of the daughtercard. Low profile card outlines are permitted provided that the mechanical integrity and placement of the faceplate mounting and connector fingers are maintained. On daughtercards which do not use the JTAG function, TDI should be jumpered to TDO to complete the JTAG chain.

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